CLAIMS:

1. An integrated circuit device comprising:

a semiconductor die;

a first housing encapsulating the semiconductor die;

a heat sink positioned proximate to the first housing; and

a second housing encapsulating at least a portion of the heat sink.

2. The integrated circuit device according to claim 1 further comprising at least one first lead coupled with the semiconductor die and the first housing encapsulates at least a portion of the at least one first lead.

3. The integrated circuit device according to claim 1 wherein the heat sink comprises:

a body; and

at least one second lead coupled with the body and the second housing encapsulates at least a portion of the at least one second lead.

4. The integrated circuit device according to claim 3 wherein the at least one second lead is configured to dissipate heat from the semiconductor die.

5. The integrated circuit device according to claim 1 wherein the second housing encapsulates a majority of the heat sink.

6. The integrated circuit device according to claim 1 wherein the second housing encapsulates a majority of the heat sink and at least a portion of the first housing.

7. The integrated circuit device according to claim 1 wherein the second housing encapsulates a majority of the heat sink and a majority of the first housing.

8. The integrated circuit device according to claim 1 wherein the semiconductor die comprises a synchronous-link dynamic random access memory device and the second housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

9. An integrated circuit device comprising:

a semiconductor die having a plurality of bond pads;

a plurality of leads electrically coupled with the bond pads of the semiconductor die;

a first housing encapsulating the semiconductor die and at least a portion of the leads;

a heat sink thermally coupled with the first housing; and

a second housing encapsulating at least a portion of the heat sink.

10. The integrated circuit device according to claim 9 wherein the heat sink comprises a metal and the first housing contacts the metal.

11. The integrated circuit device according to claim 9 wherein the heat sink includes at least one lead configured to dissipate heat from the semiconductor die.

12. The integrated circuit device according to claim 9 wherein the second housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

13. The integrated circuit device according to claim 9 wherein the second housing encapsulates the first housing.

14. An integrated circuit device comprising:

a first housing formed about a semiconductor die and at least portions of a plurality of leads electrically coupled with the semiconductor die;

a heat sink thermally coupled with the first housing; and

a second housing formed about the heat sink and at least a portion of the first housing.

15. The integrated circuit device according to claim 14 wherein the first housing and second housing individually comprise an encapsulant housing.

16. The integrated circuit device according to claim 14 wherein the heat sink contacts the first housing.

17. The integrated circuit device according to claim 14 wherein the heat sink further includes at least one lead configured to dissipate heat from the semiconductor die.

18. A synchronous-link dynamic random access memory device comprising:

a semiconductor die bearing synchronous-link dynamic random access memory circuitry and having a plurality of bond pads coupled therewith;

a plurality of leads electrically coupled with the bond pads of the semiconductor die;

a first housing encapsulating the semiconductor die and at least a portion of the leads;

a heat sink positioned proximate the first housing and configured to draw heat from the semiconductor die; and

a second housing encapsulating the heat sink and at least a portion of the first housing.

19. The synchronous-link dynamic random access memory device according to claim 18 wherein the second housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

20. The synchronous-link dynamic random access memory device according to claim 18 wherein the heat sink comprises at least one lead configured to dissipate heat from the semiconductor die.

21. A method of forming an integrated circuit device comprising:

providing a semiconductor die;

forming a first housing about the semiconductor die;

thermally coupling a heat sink with the first housing; and

forming a second housing about at least a portion of the heat sink following the thermally coupling.

22. The method according to claim 21 wherein the providing comprises providing a semiconductor die coupled with plural leads of a lead frame.

23. The method according to claim 22 further comprising bending the leads to form one of a vertical surface mounted package and a horizontal surface mounted package.

24. The method according to claim 21 wherein the forming the first housing and the forming the second housing individually comprise encapsulating.

25. The method according to claim 21 wherein the forming the second housing comprises encapsulating at least a portion of the first housing.

26. The method according to claim 21 further comprising providing the heat sink with at least one lead.

27. A method of forming an integrated circuit device comprising:

providing a semiconductor die having a plurality of bond pads;

providing a first lead frame having a plurality of leads;

providing a second lead frame having a heat sink;

electrically coupling the bond pads of the semiconductor die with the leads of the first lead frame;

first encapsulating the semiconductor die and at least a portion of the leads, the first encapsulating forming a first housing;

thermally coupling the heat sink with the first housing; and

second encapsulating at least a portion of the heat sink forming a second housing following the thermally coupling.

28. The method according to claim 27 wherein the second encapsulating further comprises encapsulating at least a portion of the first housing.

29. The method according to claim 27 wherein the second encapsulating further comprises encapsulating a majority of the heat sink and a majority of the first housing.

30. The method according to claim 27 wherein the thermally coupling comprises positioning the heat sink to contact the first housing.

31. The method according to claim 27 further comprising bending the leads to form one of a vertical surface mounted package and a horizontal surface mounted package.

32. The method according to claim 27 wherein the providing the second lead frame comprises providing the heat sink with at least one lead.

33. A method of forming an integrated circuit device comprising:

providing a semiconductor die electrically coupled with a plurality of leads;

forming a first housing about the semiconductor die and at least a portion of the leads;

providing a heat sink; and

forming a second housing about at least a portion of the heat sink, the forming the second housing thermally coupling the heat sink with the semiconductor die.

34. The method according to claim 33 further comprising positioning a heat sink proximate the first housing prior to forming the second housing.

35. The method according to claim 33 wherein the forming the first housing and the forming the second housing individually comprise encapsulating.

36. The method according to claim 33 wherein the forming the second housing comprises forming the second housing about at least a portion of the first housing.

37. The method according to claim 33 wherein the forming the second housing comprises encapsulating at least a portion of the heat sink and at least a portion of the first housing.

38. The method according to claim 33 wherein the providing the heat sink comprises providing the heat sink having at least one lead.

39. The method according to claim 33 further comprising bending the leads to form one of a vertical surface mounted package and a horizontal surface mounted package.

40. A method of forming a synchronous-link dynamic random access memory edge-mounted device comprising:

providing a semiconductor die having a plurality of bond pads;

providing a first lead frame having a plurality of leads;

providing a second lead frame having a heat sink;

electrically coupling the bond pads of the semiconductor die with the leads of the first lead frame;

positioning the semiconductor die and the first lead frame within a first mold following the electrically coupling;

first encapsulating the semiconductor die and at least a portion of the leads within the first mold using a first encapsulant;

curing the first encapsulant forming a first housing;

removing the first housing from the first lead frame;

positioning the heat sink of the second lead frame to contact a surface of the first housing;

providing the semiconductor die and the second lead frame within a second mold following the positioning the heat sink;

second encapsulating the first housing and the heat sink within the second mold using a second encapsulant;

curing the second encapsulant forming a second housing;

removing the second housing from the second lead frame;

trimming the leads; and

bending the leads to form one of a vertical surface mounted package and a horizontal surface mounted package.